ULTRA HIGH-SPEED DDP-SRAM CACHE

ABSTRACT OF THE DISCLOSURE

An ultra high-speed DDP-SRAM (Dual Dual-Port Static Random Access Memory) cache having a cache speed in approximately the GHz range. This is accomplished by (1) a specially designed dual-port SRAM whose size is slightly larger than that of a conventional single port SRAM, and (2) the use of a dual dual-port SRAM architecture which doubles its speed by interleaved read and write operations. A first embodiment provides a 6-T (transistor) all nMOS dual-port SRAM cell. A second embodiment provides a dual port 7T-SRAM cell which has only one port for write, and both ports for read.